Hexagonal a-Si:H TFTs: A New Advanced Technology for Flat-Panel Displays

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***Abstract*—Inverted stagger hexagonal hydrogenated amorphous silicon thin-film transistors (a-Si:H HEX-TFTs) were fabricated with a five-photomask process used in the processing of the active-matrix liquid crystal displays. We show that the output current of a-Si:H HEX-TFTs connected in parallel increases linearly with their number within a given pixel circuit. Current–voltage measurements indicate that a high ON–OFF current ratio and a low subthreshold slope can be maintained for multiple HEX-TFTs connected in parallel, whereas the field-effect mobility and threshold voltage remain identical to a single a-Si:H HEX-TFT. Due to a unique device geometry, an enhanced electrical stability and a larger pixel aperture ratio can be achieved in the multiple a-Si:H HEX-TFT in comparison to a standard single a-Si:H TFT having the same channel width. These HEX-TFT electrical characteristics are very desirable for active-matrix organic light-emitting displays.**

***Index Terms*—Hexagonal thin-film transistor (HEX-TFT), hydrogenate amorphous silicon (a-Si:H), large channel width, multiple transistor, parallel connected.**

I. Introduction

Due to the spatial uniformity and simple processing, the hydrogenate amorphous silicon thin-film transistor (a-Si:H TFT) has been widely used over the last ten years as an active-matrix array backplane for large-area flat-panel displays and imaging arrays. However, at the same time, due to its low carrier field-effect mobility, the a-Si:H TFT is suffering from a low drain current for a given gate/drain bias, which becomes a critical factor for a driving TFT in active-matrix organic light-emitting devices (AM-OLEDs) or in-plane gate drivers [1] for flat-panel displays. In the a-Si:H TFT, a high drain current can be achieved by simply increasing the channel width for a given length using normal source/drain (S/D) electrodes, comb-shaped electrodes [2], or fork-shaped electrodes [3]. However, it is known that a single transistor with the increased channel width results in a serious TFT threshold voltage variation [4], [5]. Alternatively, a Corbino a-Si:H TFT [6] structure can be employed; its unique asymmetric ring-shaped electrode enables to achieve a high output current and provides a better electrical stability by eliminating the sharp corner present in classical devices. However, due to the area limits in pixel electrodes and its unique electrode shape, the channel width of the Corbino a-Si:H TFT as a single transistor cannot be enlarged enough to achieve a high current, which is required for high-resolution flat-panel displays or in-plane gate drivers.

In this paper, to address the aforementioned issues, we are proposing for the first time parallel-connected hexagonal a-Si:H TFTs (a-Si:H HEX-TFTs) for a given pixel circuit to achieve a high stable output current over time. We choose the hexagonal shape for the multiple a-Si:H TFT structure since it represents an optimum shape to minimize the areal occupation when TFTs are integrated together in parallel in a given circuit. At the same time, we also expect that the multiple a-Si:H HEX-TFT structure can achieve a higher output drain current with better electrical stability in comparison to other single a-Si:H TFT structures. First, we report on the electrical characteristics of the single and multiple a-Si:H HEX-TFTs. More specifically, we describe the effects of the parallel connection of single HEX-TFTs on the overall device performance. We also discuss the impact of the number of HEX-TFTs on the extracted key device electrical parameters such as the subthreshold slope (SS), field-effect mobility, and threshold voltage, which are important for active-matrix liquid crystal displays (AM-LCDs) and AM-OLEDs. Then, we compare electrical properties of the multiple HEX-TFT connected in parallel with the standard single a-Si:H TFT having different equivalent channel widths. Finally, we present electrical stabilities and pixel aperture ratio of the multiple HEX-TFT in a given pixel area in comparison to the single standard a-Si:H TFT. To our best knowledge, this paper represents the first investigation of the electrical characteristics of single and multiple a-Si:H HEX-TFTs and their proposed application to flat-panel displays. We consider this paper as an introduction to a new advanced a-Si:H TFT technology for future flat-panel displays.

II. Multiple a-Si:H HEX-TFT Structure and Fabrication

In this paper, a series of a-Si:H TFTs connected in parallel, with a gate length of 5 μm, consisting of octuple HEX-TFTs (HEX-8), quadruple HEX-TFTs (HEX-4), double HEX-TFTs (HEX-2), and a single HEX-TFT (HEX-1), was fabricated, as listed in Table I. All HEX-TFT structures were constructed of identical single a-Si:H HEX-TFTs as a base unit, and all gate, drain, and source electrodes of the a-Si:H HEX-TFTs are connected in parallel, respectively (Fig. 1). The single

Manuscript received June 12, 2007; revised October 9, 2007. This work was supported by the Research and Development Center, LG Philips LCD, Korea. The review of this paper was arranged by Editor H.-S. Tae.

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Digital Object Identifier 10.1109/TED.2007.911090

TABLE I
DEVICE DIMENSIONS OF VARIOUS MULTIPLE a-Si:H HEX-TFTs

Device Name	Channel Length (L)	Number of Multiple TFT	Effective Channel Width (W_{EFF})	
			Linear	Saturation
Hex-1	5 μm	1	285 μm	300 μm
Hex-2	5 μm	2	570 μm	600 μm
Hex-4	5 μm	4	1140 μm	1200 μm
Hex-8	5 μm	8	2280 μm	2400 μm

$W_{EFF\text{-}Linear}$ = Number of HEX-TFT × 6 × (R_1 + L/3$^{1/2}$)

$W_{EFF\text{-}Saturation}$ = Number of HEX-TFT × 6 × R_2

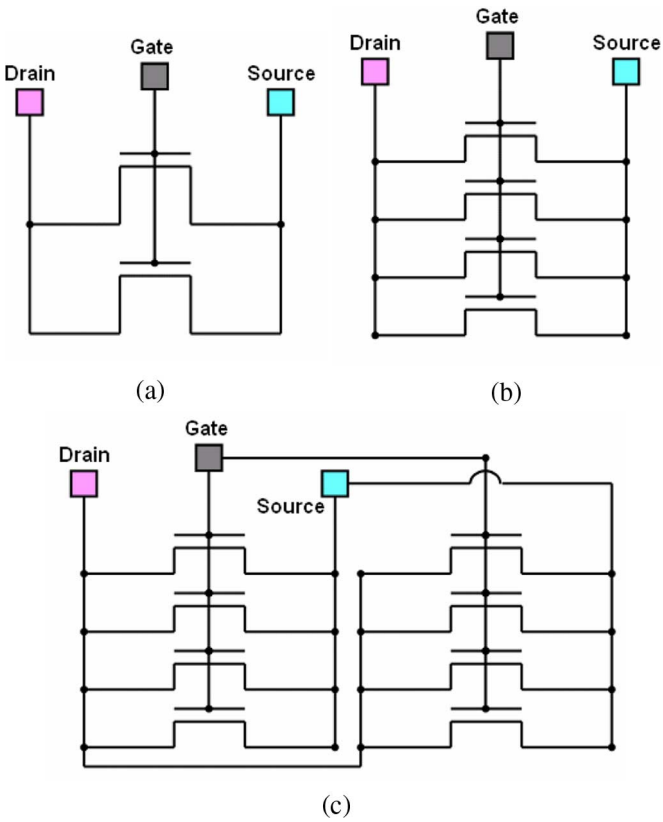


Fig. 1. Schematics of a-Si:H HEX-TFTs connected in parallel. (a) HEX-2. (b) HEX-4. (c) HEX-8.

a-Si:H HEX-TFT consists of an inner hexagonal electrode (outer side length $R_1 = 44$ μm) and an outer ring-shaped hexagonal electrode (inner side length $R_2 = 50$ μm) (Fig. 2). The bottom-gate electrode is large enough to cover the entire area of the device outer and inner electrodes. Fig. 2(b) presents the cross section of a single a-Si:H HEX-TFT structure. All multiple a-Si:H HEX-TFTs were fabricated using the normal AM-LCD five-photomask process steps [7]. More specifically, on the Corning EAGLE2000 glass substrate, a bilayer of aluminum–neodymium compound (AlNd, 2000 Å) and molybdenum (Mo, 500 Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet etching (mask 1). After gate electrode definition, a hydrogenated amorphous silicon nitride (a-SiN$_X$:H, 4000 Å)/

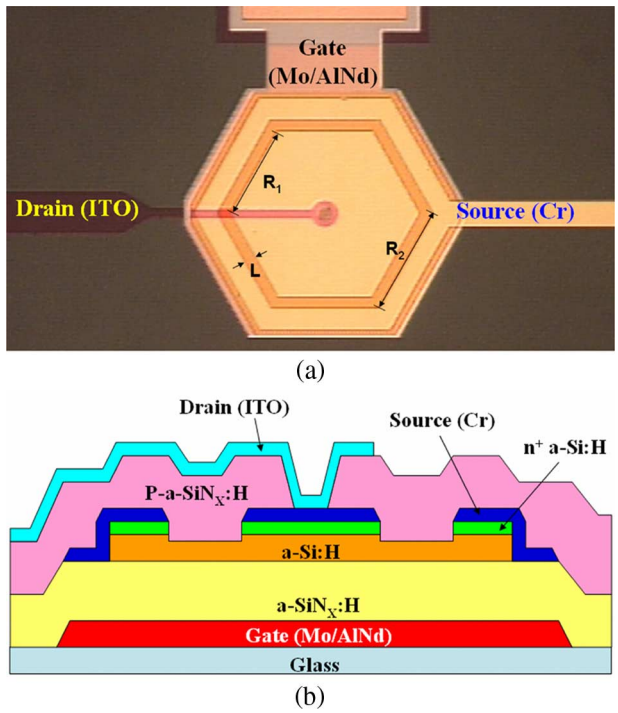


Fig. 2. (a) Top and (b) cross-sectional views of a single a-Si:H HEX-TFT device.

a-Si:H (1700 Å)/phosphorous-doped a-Si:H (n$^+$ a-Si:H, 300 Å) trilayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form a gate insulator and an active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (mask 2), a chromium (Cr, 1200 Å) layer was deposited by sputtering, and S/D electrodes were patterned by wet etching (mask 3). Using S/D metal and photoresist as masks, back-channel etching by RIE was performed. Then, we deposited a-SiN$_X$:H (3000 Å) as a passivation layer by PECVD at 300 °C. To make a contact for the pixel electrode indium tin oxide (ITO), a via was formed through the passivation (phosphorus-doped vapor-deposited oxide) layer by RIE (mask 4). After contact via definition, ITO (500 Å) was deposited by a sputtering method at room temperature, and then, pixel electrodes were patterned by wet etching (mask 5). As a final step, the device thermal annealing was performed for an hour at 235 °C; this step is needed to improve the optical and electrical properties of ITO. It should be noted that all fabricated HEX-TFTs were not considered for minimizing the area occupation in the pixel circuit, and this issue will be discussed later in Section III-B.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Electrical Characteristics of Multiple a-Si:H HEX-TFTs

To characterize the electronic properties of multiple HEX-TFTs connected in parallel, we first measured the output characteristics for different configurations (Fig. 3). We have shown in the previous study that the Corbino a-Si:H TFT [6] with asymmetric electrode geometry could have different

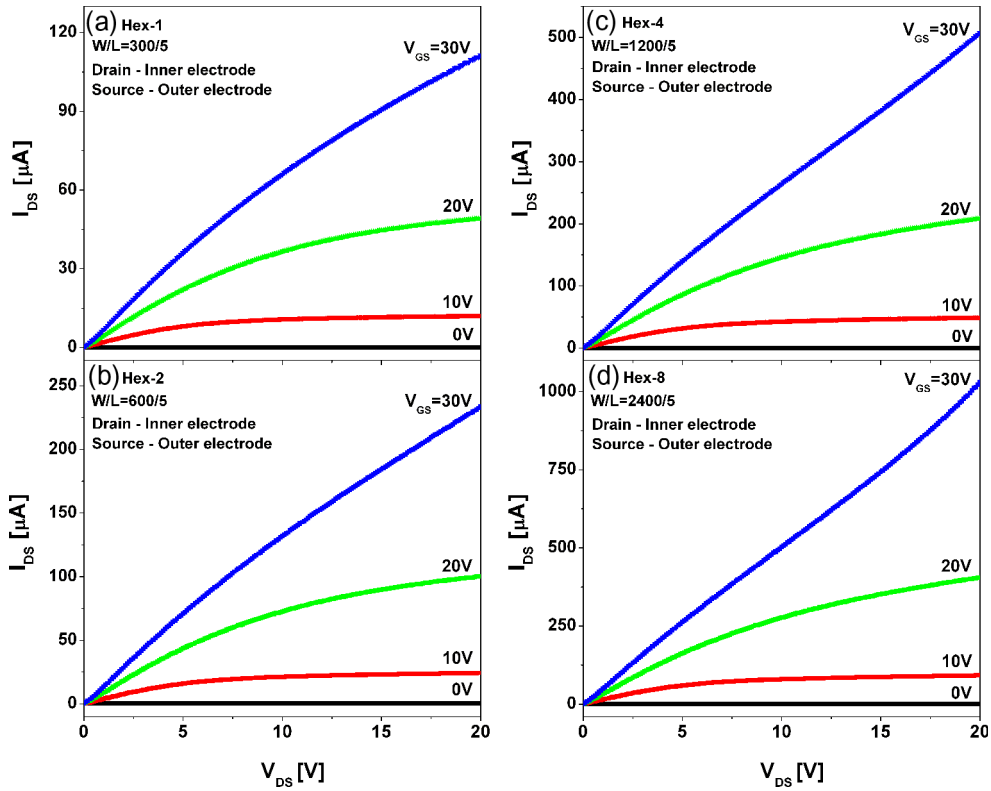


Fig. 3. Output characteristics of multiple a-Si:H HEX-TFTs. (a) HEX-1 (b) HEX-2. (c) HEX-4. (d) HEX-8.

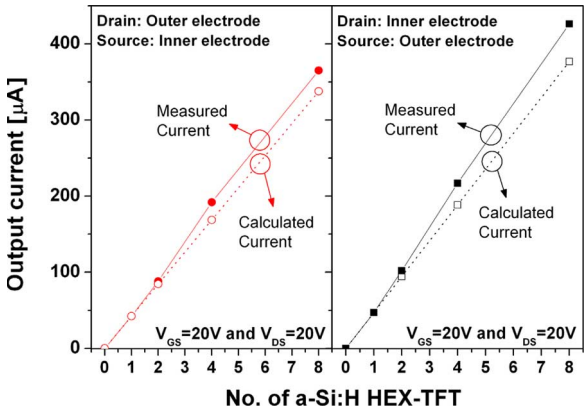


Fig. 4. Measured (closed symbol) and calculated (open symbol) output current values of multiple a-Si:H HEX-TFTs at $V_{\rm GS} = 20$ and $V_{\rm DS} = 20$ V as a function of the number of HEX-TFTs. (a) Drain is applied on the inner electrode, whereas source is applied on the outer electrode. (b) Drain is applied on the outer electrode, whereas source is applied on the inner electrode.

electrical properties depending on the drain bias condition. In this paper, we fixed the drain bias condition to achieve the highest output drain current level by applying the drain bias on the inner hexagonal electrode and the source (ground) on the outer ring-shaped hexagonal electrode (Fig. 3). We swept the drain bias from 0 to 20 V for various gate voltages (0, 10, 20, and 30 V), and the output current of multiple a-Si:H HEX-TFTs increases linearly with the increasing number of a-Si:H HEX-TFT units in parallel, following (1). To check the linearity of the total output current with the number of HEX-TFTs, we calculated the total output current value for different multiple a-Si:H HEX-TFT configurations by multiplying the number of HEX-TFTs by the output current of a single a-Si:H HEX-TFT measured at $V_{\rm GS} = 20$ V and $V_{\rm DS} = 20$ V, and we compared the calculated values with the actual output current values of multiple a-Si:H HEX-TFTs measured at $V_{\rm GS} = 20$ V and $V_{\rm DS} = 20$ V (Fig. 4). As shown in this figure, the measured output current values are only slightly highe ($> 10\%$) than the calculated values, but show a very good linearity with the number of multiple HEX-TFTs for both drain bias conditions. Thus

$$I_{\rm out}^{\rm Total} \geq \sum_i I_{\rm out}^i \tag{1}$$

where $I_{\rm out}^{\rm Total}$ is the total output current for multiple HEX-TFTs, and $I_{\rm out}^i$ is the output current for a single HEX-TFT used in a parallel-connected circuit. To verify this relationship, we measured the output current for different bias conditions ($V_{\rm DS} = 5$, 10, and 15 V), and the good linearity of output current was still observed with the number of multiple HEX-TFTs. Therefore, in this unique advanced a-Si:H TFT technology, a desirable output current level can be obtained by adjusting the number of HEX-TFTs used in a given pixel circuit. For example, to achieve a desirable output current of 200 μA for the a-Si:H TFT AM-OLED, we will need four of HEX-TFTs (HEX-4) connected in parallel.

Fig. 5 shows the transfer characteristics of multiple a-Si:H HEX-TFTs; we swept the gate bias from -10 to 20 V for various drain voltages (0.1, 10, and $V_{\rm SAT}$), where $V_{\rm SAT}$ is the drain voltage $V_{\rm DS}$ when the drain is connected to the gate electrode to keep the transistor in a saturation regime

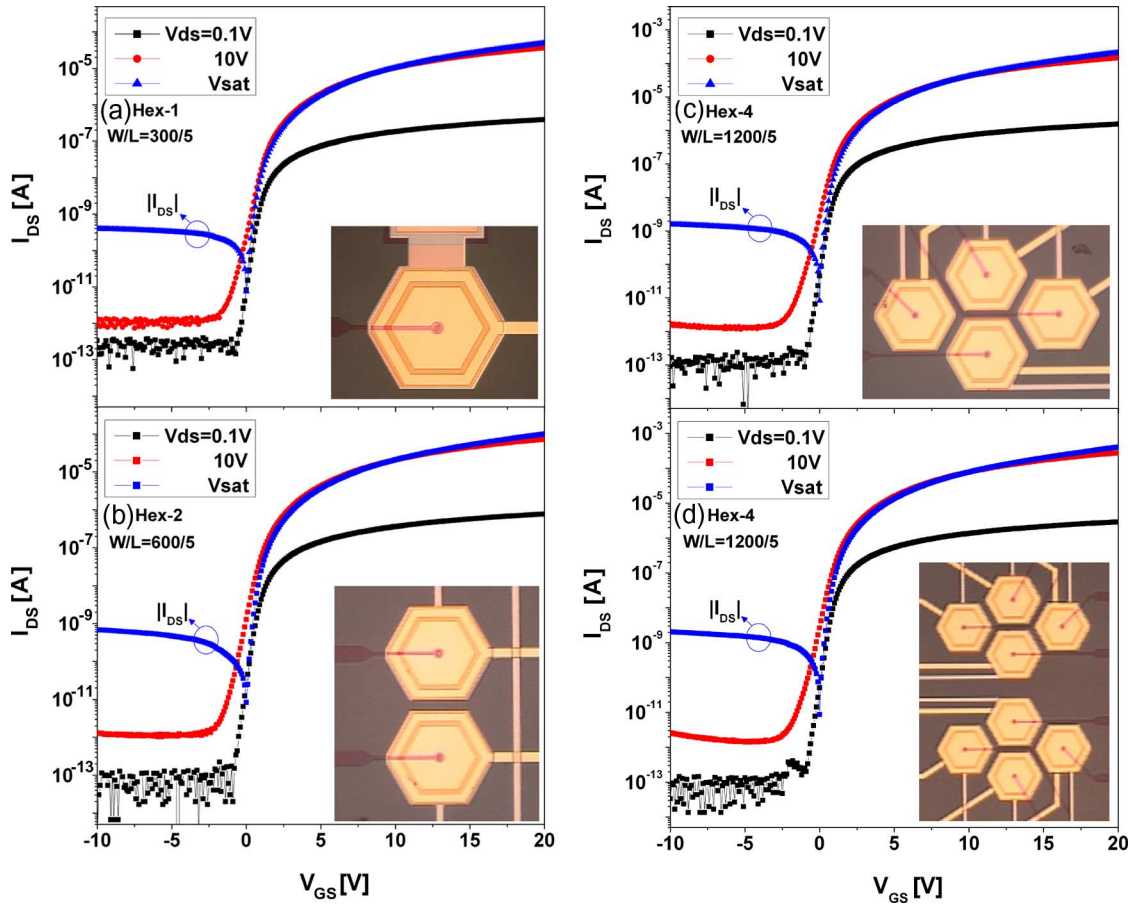


Fig. 5. Transfer characteristics and top views of multiple a-Si:H HEX-TFTs, where $|I_{\rm DS}|$ represents the negative $I_{\rm DS}$ value. (a) HEX-1. (b) HEX-2. (c) HEX-4. (d) HEX-8.

($V_{\rm DS} = V_{\rm GS} > V_{\rm GS} - V_{\rm TH}$). In Fig. 5(a), for $V_{\rm DS} = 0.1$ V and $V_{\rm SAT}$, a single a-Si:H HEX-TFT shows SS values of 348 and 160 mV/dec, respectively, and OFF current levels of 2.0×10^{-13} and 8.5×10^{-13} A, respectively. Here, the subthreshold swings for the linear and saturation regimes of operation are defined as the inverse values of the steepest slopes of the respective $I_{\rm DS}$–$V_{\rm GS}$ semilog plots. By comparing the electrical properties of multiple HEX-TFTs, the transfer characteristics reveal that the HEX-8 TFT [Fig. 5(d)] has the highest ON/OFF ratio of 8.7×10^{7} at $V_{\rm DS} = 0.1$ V and the smallest SS of 126 mV/dec at $V_{\rm DS} = V_{\rm SAT}$. It should be noted that when $V_{\rm DS} = V_{\rm SAT}$, $I_{\rm DS}$ becomes negative as $V_{\rm GS}$ changes to negative values. For this measurement condition, the drain and gate nodes are connected together. Therefore, when the gate bias becomes negative, the drain node also becomes negative. As a result, the potential at the drain node becomes lower than that at the source node, and the current starts flowing from the source node to the drain node (negative current). As shown in Fig. 6(a), the SS for both $V_{\rm DS} = 0.1$ V and $V_{\rm SAT}$ decreases with the increasing number of a-Si:H HEX-TFTs from HEX-1, HEX-2, and HEX-4, to HEX-8, whereas the OFF current at $V_{\rm DS} = 0.1$ and 10 V remains at the similar level within the error range regardless of the increasing number of HEX-TFTs. It is important to mention that all values presented are means of several separate measurements, and the error bars stand for the standard deviation for these values.

Fig. 6(b) shows the variation of the threshold voltage $V_{\rm TH}$ and the field-effect mobility $\mu_{\rm FE}$ as a function of the number of a-Si:H HEX-TFTs. We extracted the field-effect mobility μ and the threshold voltage by using the maximum slope method [6], [8], which is usually used for crystalline silicon devices. In this method, the field-effect mobility is calculated from the transconductance maximum ($g_m = dI_{\rm DS}/dV_{\rm GS}$) value using the following equations:

$$\mu_{\rm Linear} = \frac{g_{\rm m\text{-}Linear} \cdot L}{W_{\rm EFF1} C_{\rm OX} V_{\rm DS}} \tag{1a}$$

$$\mu_{\rm Saturation} = \frac{g_{\rm m\text{-}Saturation^2} \cdot 2L}{W_{\rm EFF2} C_{\rm OX}} \tag{1b}$$

where $g_{\rm m\text{-}Linear}$ is the maximum transconductance at $V_{\rm DS} = 0.1$ V, and $g_{\rm m\text{-}Saturation}$ is the maximum transconductance at $V_{\rm DS} = V_{\rm SAT}$. From the value of $V_{\rm GS}$ corresponding to g_m as a reference, two closest different gate bias values are chosen so that the straight fitting line is drawn based on these three points in the transfer characteristic curves. The threshold voltage is estimated from the x-axis intercept of this extrapolated line for each drain bias condition. Based on our previous investigation of the geometrical effect on the a-Si:H TFT characteristics [6], the effective channel widths $W_{\rm EFF1}$

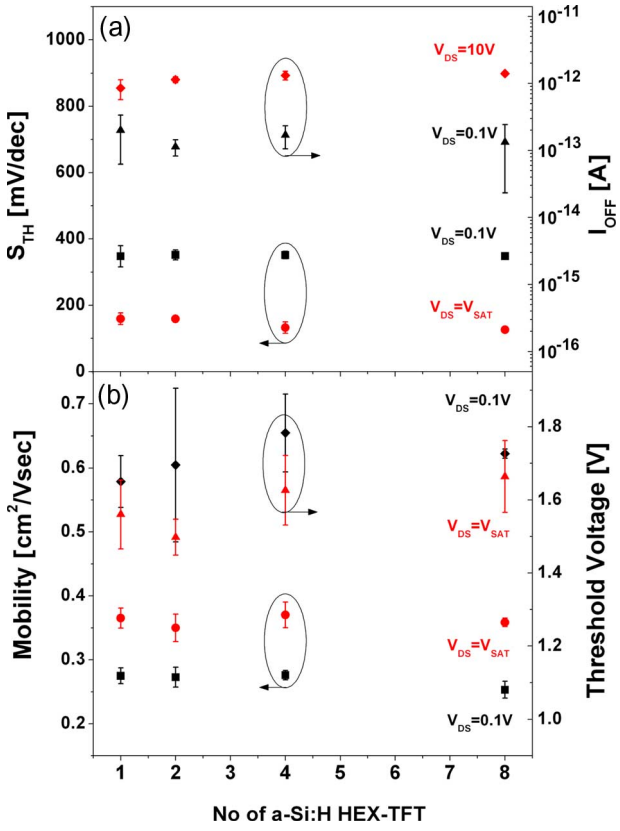


Fig. 6. Trends of the (a) subthreshold swing and OFF current and (b) field-effect mobility and threshold voltage of multiple a-Si:H HEX-TFTs as a function of the number of TFTs.

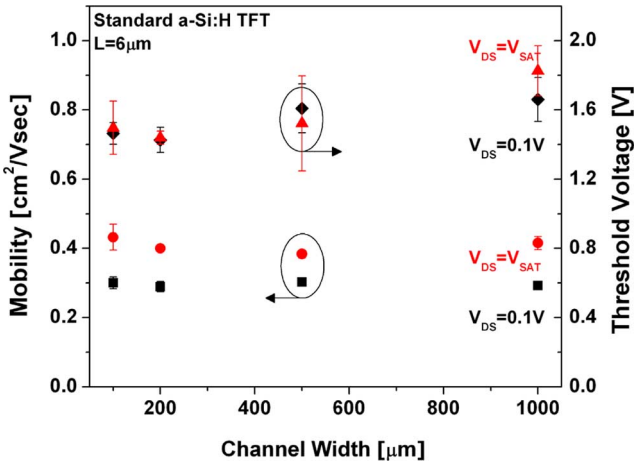


Fig. 7. Trend of the field-effect mobility and threshold voltage of a standard TFT as a function of different channel widths.

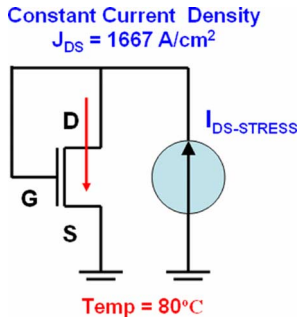


Fig. 8. Schematics of the CTS measurement setup used for standard and multiple a-Si:H HEX-TFTs.

and W_{EFF2} for each drain bias condition are calculated by the following equations:

$$W_{\mathrm{EFF1}} = \text{Number of a-Si:H HEX-TFTs} \times 6 \times \left(R_1 + \frac{L}{\sqrt{3}}\right) \quad (2a)$$

$$W_{\mathrm{EFF2}} = \text{Number of a-Si:H HEX-TFTs} \times 6 \times R_2 \quad (2b)$$

where W_{EFF1} is the effective channel width for the linear regime operation ($V_{\mathrm{DS}} = 0.1$ V), and W_{EFF2} is the effective channel width for the saturation regime operation ($V_{\mathrm{DS}} = V_{\mathrm{GS}} = V_{\mathrm{SAT}}$). Experimental results reveal that HEX-1, HEX-2, HEX-4, and HEX-8 a-Si:H TFTs yield almost the same field-effect mobility and threshold voltage values within the error range, indicating that the field-effect mobility and threshold voltage are not affected by the numbers of HEX-TFTs connected in parallel. Such TFT connection will allow increasing the overall device channel width and output current at the same time. For comparison, we also fabricated standard a-Si:H TFTs with different channel widths of 100, 200, 500, and 1000 μm and with channel length $L = 5$ μm. The field-effect mobility and threshold voltage values were calculated using the same method. As shown in Fig. 7, for standard a-Si:H TFTs, the field-effect mobility does not change, but the threshold voltage increases with the increasing channel width. Others made a similar observation [9]. Hence, we expect that the threshold voltage increase will be more severe if the channel width increases to a value higher than 1000 μm to be comparable to the total width of HEX-4 or HEX-8 a-Si:H TFT (Table I). It should be noted again that all values presented are means of several separate measurements, and the error bars stand for the standard deviation for these values.

B. Electrical Stabilities and Pixel Area Occupation of Multiple a-Si:H HEX-TFTs

To evaluate the thermal and electrical stabilities of the multiple a-Si:H HEX-TFTs for AM-OLEDs, we performed the current–temperature stress (CTS) experiment for HEX-2 and HEX-4 a-Si:H TFTs. For comparison, we chose the standard a-Si:H TFT with $W/L = 1000/6$ and performed the same CTS experiment. For the CTS measurement, we connected the gate and drain of the TFT together and continuously applied the constant current through the drain to the TFT while the source was set to ground (Fig. 8). In this set up, we can avoid the gate bias stress and only investigate the drain current stress on the device. For the HEX-TFT structure, the drain current stress is applied on the inner electrode, and the source is connected to the outer ring-shaped electrode. Since all TFTs used in experiments have different W/L ratios, we applied different drain current levels depending on their channel width to maintain the same stress current density ($J_{\mathrm{DS}} = I_{\mathrm{DS}}/(W \times t_{\mathrm{CH}}) = 1667$ A/cm^2), which corresponds to the drain current of 100,

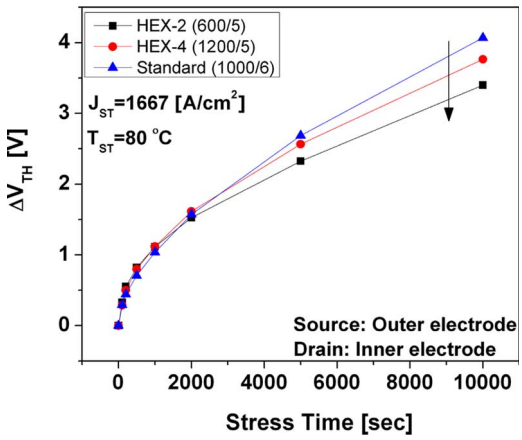


Fig. 9. Variations of the threshold voltage of the HEX-2 and HEX-4 a-Si:H TFTs as a function of stress time at 80 °C in comparison to a standard a-Si:H TFT.

200, and 167 μA for the HEX-2 ($W/L = 600/5$), HEX-4 ($W/L = 1200/5$), and standard ($W/L = 1000/6$) a-Si:H TFTs, respectively. In calculating the channel current density, we assume that its thickness $t_{\rm CH}$ is the same, i.e., 10 nm, for all TFT structures. The stress current density stress of 1667 A/cm^2 was determined to achieve the drain current of 100 μA for the HEX-2 a-Si:H TFT at $V_{\rm DS} = V_{\rm GS} = 20$ V, which corresponds to the OLED luminance of 10 000 cd/m^2 for the emission efficiency of 3.0 cd/A and the pixel size of 300×100 μm^2. All CTS measurements were performed under the accelerated stress condition by setting the stress temperature $T_{\rm ST}$ at 80 °C. We measured the transfer characteristics of TFTs with $V_{\rm DS} = V_{\rm SAT}$ (connected to the gate bias) at the stress temperature (80 °C) for different stressing times $t_{\rm ST}$ ranging from 0 to 10 000 s. We only stopped device stressing for about 60 s to measure the transfer curves between different stress times. From the transfer characteristics, the threshold voltages are extracted by the maximum slope method [8] for different stressing times. As the stressing time increases from 0 to 10 000 s, the threshold voltage shift $\Delta V_{\rm TH}$ of the standard a-Si:H TFT increases from 0 to 4.1 V, whereas the $\Delta V_{\rm TH}$ of HEX-2 and HEX-4 increase from 0 to 3.4 V and 0 to 3.8 V, respectively (Fig. 9). It means that for the same stress current density, the TFT threshold voltage shift for 10 000 s is reduced by 19.7% for the HEX-2 TFT ($W/L = 600/5$) in comparison to the standard TFT ($W/L = 1000/6$). Even for the HEX-4 TFT with a larger W/L ratio (i.e., 1200/5), the threshold voltage shift is still smaller by 8.1% for 10 000 s. Therefore, parallel-connected multiple HEX-TFTs have an enhanced electrical stability in comparison to a single standard TFT with a similar W/L ratio.

It can be easily realized from the honeycomb structure that the hexagonal shape is very desirable in reducing the pixel area occupational space. Hence, by arranging the single a-Si:H HEX-TFT in a desirable way, we can expect a tremendous reduction in the pixel area occupation for a given circuit design. Fig. 10 shows the layouts of the standard TFT, the interdigitated electrode TFT, and the proposed HEX-4 TFT with the same channel width and length ($W/L = 330/6$). All layouts

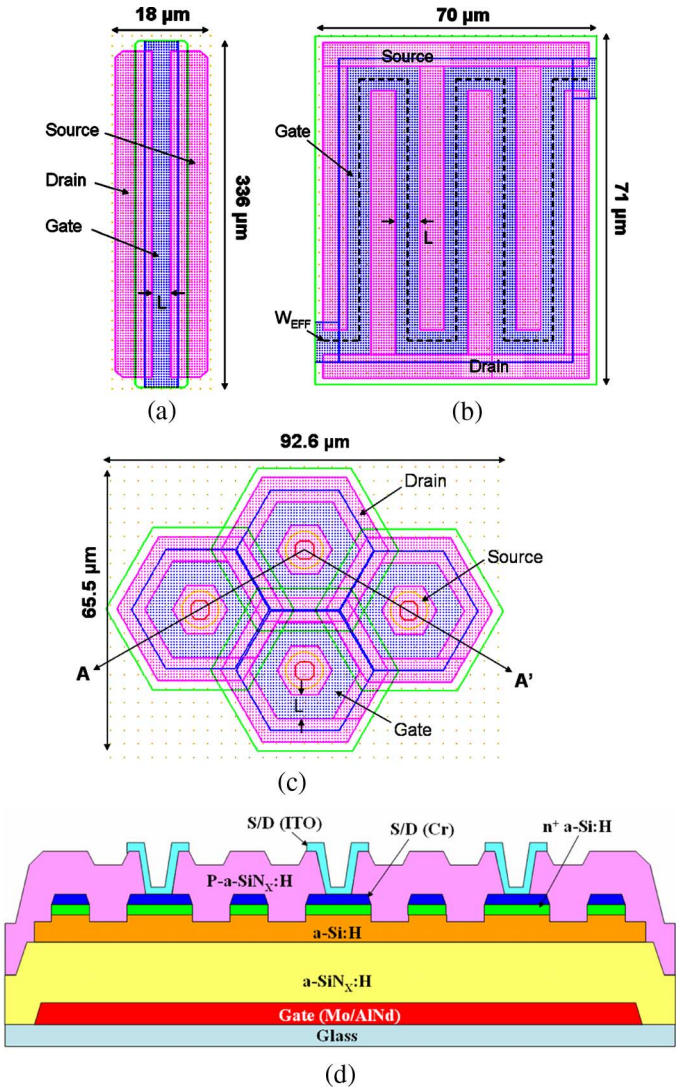
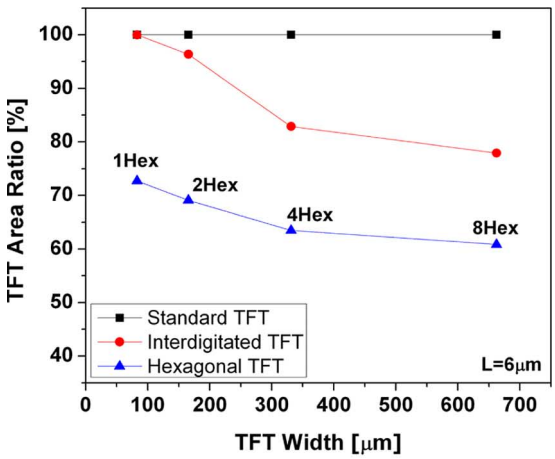
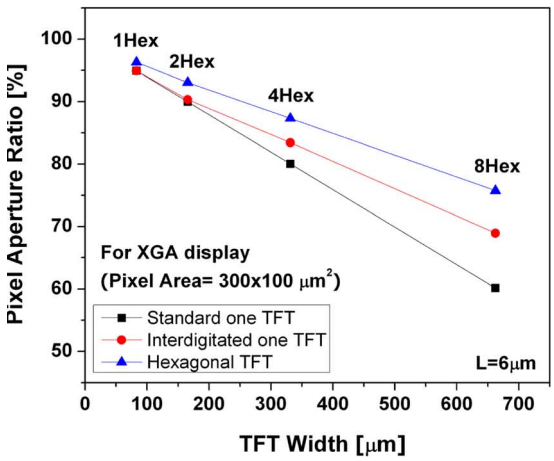


Fig. 10. Layouts of the (a) standard TFT, (b) interdigitated electrode TFT, and (c) our proposed HEX-4 TFT with the same channel width and length ($W/L = 330/6$). All layouts were drawn in Virtuoso layout environment. (d) Cross-sectional schematic of the proposed HEX-4 a-Si:H TFT.

were drawn in Virtuoso layout environment using a-Si:H TFT array process design rules, and their respective channel width and length are kept the same. For simplicity, we draw only electrodes of the gate and S/D without signal connection lines. Then, we calculated the area of each TFT from the layout. Fig. 10(d) shows the cross-sectional schematic of the proposed HEX-4 a-Si:H TFT. The same methodology was applied to other HEX-TFT structures (HEX-1, HEX-2, and HEX-8) and the corresponding standard and interdigitated electrode TFTs. It should be noted that the size of the inner electrode of all a-Si:H HEX-TFTs decreases to minimize the pixel area occupation and overlap parasitic capacitance. As shown in Fig. 11(a), the pixel area occupation ratio is reduced by 37% for the HEX-4 TFT in comparison to a standard TFT with the same W/L ratio, whereas the a-Si:H TFT with the interdigitated electrode shows a reduction of 17%. This reduction in the pixel area occupation becomes much larger from 27% to 39% as the number of HEX-TFTs increases. Fig. 11(b) shows the variation of a pixel



(a)



(b)

Fig. 11. Variations of the (a) TFT area occupation ratios and (b) pixel aperture ratios of the proposed multiple a-Si:H HEX-TFTs in comparison to an interdigitated electrode and a standard a-Si:H TFTs. TFT area occupation is defined as the area occupied by the gate and S/D electrodes of the TFT. Pixel aperture ratio is defined as the ratio between the transmissive portion of a pixel and its surrounding opaque electronics for a given pixel area.

aperture ratio as a function of channel width for different TFT structures in extended graphics array display, where the pixel area is 300×100 μm^2. The pixel aperture ratio is the ratio between the transmissive portion of a pixel and its surrounding opaque electronics (e.g., the TFTs), which is expressed as a percentage. In the standard TFT, as the channel width increases, the pixel aperture ratio decreases from 95% to 60.1%, whereas the multiple HEX-TFT-based pixel only shows a small decrease from 95% to 76%. Therefore, as the device size becomes larger to achieve a higher current needed for AM-OLEDs, a multiple HEX-TFT structure has a higher probability for a given design in achieving a larger pixel aperture ratio. In addition, since the overlapped area between the source and gate electrodes in the multiple HEX-TFTs is much smaller than in the standard or interdigitated electrode a-Si:H TFTs with the same channel width, we can expect a reduced RC delay and a kickback voltage in display. For example, if we use a HEX-4 TFT with a W/L ratio of 330/5, the overlapped area between the source and gate electrodes is only 241 μm^2, whereas the standard and interdigitated TFTs have overlapped areas of 660 and 812 μm^2, respectively, with the same W/L ratio. Based on the previously published results on the Corbino a-SI:H TFT [6], the overlapped area between the source and gate electrodes in the HEX-TFT can also be reduced by patterning the gate electrode beneath the source electrode into a ring shape. Therefore, a minimal overlapped area between gate and source electrodes can be achieved in the multiple HEX-TFTs.

Considering the excellent electrical properties of parallel-connected a-Si:H HEX-TFTs, we expect that this new advanced a-Si:H TFT technology is suitable for driving TFTs to be used in future AM-OLED or gate drivers [1], which require high ON current levels and adequate electrical stability. In addition, by substituting one standard a-Si:H TFT with a large channel width by multiple HEX-TFTs with a smaller channel width connected in parallel, we showed that a better electrical stability and a much smaller pixel area occupation can be achieved for these new devices to be used for future flat-panel displays.

IV. Conclusion

In this paper, we studied the electrical properties of single and multiple a-Si:H HEX-TFTs connected in parallel. As the number of a-Si:H HEX-TFTs increases, the overall output drain current linearly increases with their number per circuit while the SS decreases. At the same time, the OFF current, threshold voltage, and field-effect mobility of multiple a-Si:H HEX-TFTs remain the same regardless of the number of devices connected in parallel within a given pixel circuit.

Due to a high ON current, stable field-effect mobility, and threshold voltage, a parallel-connected a-Si:H HEX-TFT represents a new a-Si:H technology that can be used to realize high-performance electrically stable driving TFTs for future AM-OLEDs and a gate driver for a-Si:H TFT-based flat-panel displays. The required output current levels can be easily adjusted and controlled by choosing a desirable number of a-Si:H HEX-TFTs per pixel circuit. Finally, we expect that due to a unique device geometry, the multiple a-Si:H HEX-TFTs show an enhanced electrical stability and a larger pixel aperture ratio in comparison to a standard single a-Si:H TFT having the same large channel width. These properties are required for future success of the a-Si:H TFTs in more advanced flat-panel displays.

Acknowledgment

The authors would like to thank A. Kuo, University of Michigan, for useful discussions about a-Si:H TFT electrical measurements. All devices were invented and designed at the University of Michigan within the group of Prof. J. Kanicki. Device processing was done at the Research and Development Center, LG Philips LCD. All electrical measurements were done at the Organic and Molecular Electronics Laboratory (www.eecs.umich.edu/omelab), Department of Electrical Engineering and Computer Science, University of Michigan. To protect the IP of this new advanced a-Si:H TFT technology, several patents have been applied.

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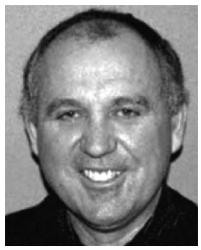

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